

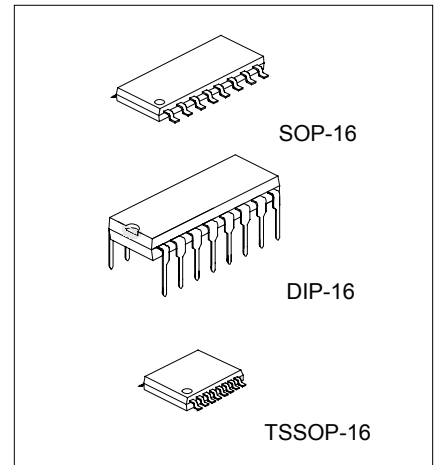
ANALOG MULTIPLEXERS/ DEMULTIPLEXERS

DESCRIPTION

The UTC 4053 are Triple SPDT analog multiplexers for application as digitally-controlled analog switches.

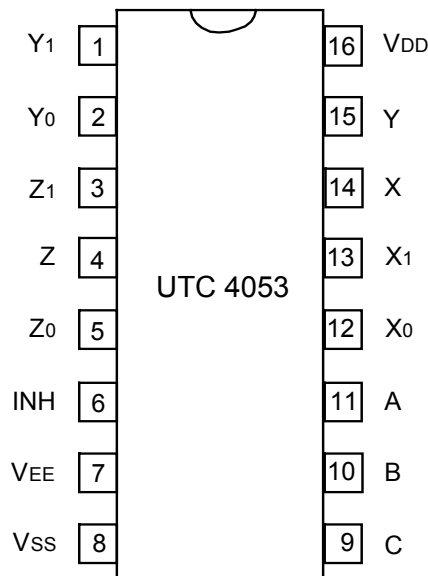
FEATURES

- * Analog Voltage Range ($V_{DD} - V_{EE}$) = 3.0 ~ 18 V
Note: V_{EE} must be $\leq V_{SS}$
- * Linearized Transfer Characteristics
- * Pin-to-Pin Replacement for CD4053

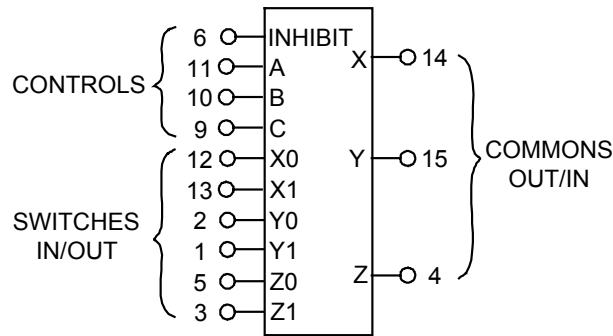


*Pb-free plating product number: 4053L

PIN CONFIGURATIONS



UTC 4053 Triple 2-Channel Analog Multiplexer/Demultiplexer



V_{DD} = PIN 16
 V_{SS} = PIN 8
 V_{EE} = PIN 7

Note: Control Inputs referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Referenced to V _{EE} , V _{SS} ≥ V _{EE})	V _{DD}	-0.5 ~ +18.0	V
Input or Output Voltage (DC or Transient) (Referenced to V _{SS} for Control Inputs and V _{EE} for Switch I/O)	V _{in} , V _{out}	-0.5 ~ V _{DD} + 0.5	V
Input Current (DC or Transient), per Control Pin	I _{in}	±10	mA
Switch Through Current	I _{SW}	±25	mA
Power Dissipation. Per Package**	P _D	500	mW
Storage Temperature	T _{stg}	-65 ~ +150	°C
Lead Temperature (8 - Second Soldering)	T _{Lead}	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

** Temperature Derating: "DIP and SOP" Packages: - 7.0 mW/°C From 65°C ~ 125°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})						
Power Supply Voltage Range	V _{DD}	V _{DD} - 3.0 ≥ V _{SS} ≥ V _{EE}	3.0		18	V
Quiescent Current per Package	I _{DD}	Control Inputs: V _{in} = V _{SS} or V _{DD} Switch I/O: V _{EE} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500mV* V _{DD} =5.0V V _{DD} =10V V _{DD} =15V		0.005 0.010 0.015	5.0 10 20	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	T _a =25°C only (The channel component, (V _{in} - V _{out})/R _{on} , is not included.) V _{DD} =5.0V V _{DD} =10V V _{DD} =15V		(0.07 μA/kHz) f + I _{DD} Typical (0.20 μA/kHz) f + I _{DD} (0.36 μA/kHz) f + I _{DD}		μA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V_{SS})						
Low – Level Input Voltage	V _{IL}	R _{on} = per spec, I _{off} = per spec V _{DD} =5.0V V _{DD} =10V V _{DD} =15V		2.25 4.50 6.75	1.5 3.0 4.0	V
High – Level Input Voltage	V _{IH}	R _{on} = per spec, I _{off} = per spec V _{DD} =5.0V V _{DD} =10V V _{DD} =15V	3.5 7.0 11	2.75 5.50 8.25		V
Input Leakage Current	I _{in}	V _{in} = 0 or V _{DD} , V _{DD} =15V		±0.00001	±0.1	µA
Input Capacitance	C _{in}			5.0	7.5	pF
SWITCHES IN/OUT AND COMMONS OUT/IN -- X, Y, Z (Voltages Referenced to V_{EE})						
Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	Channel On or Off	0		V _{DD}	V _{PP}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 3)	ΔV _{switch}	Channel On	0		600	mV
Output Offset Voltage	V _{OO}	V _{in} = 0V, No Load		10		µV
ON Resistance	R _{on}	ΔV _{switch} ≤ 500mV* V _{in} = V _{IL} or V _{IH} (Control), and V _{in} = 0 to V _{DD} (Switch) V _{DD} =5.0V V _{DD} =10V V _{DD} =15V		250 120 80	1050 500 280	Ω
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	V _{DD} =5.0V V _{DD} =10V V _{DD} =15V		25 10 10	70 50 45	Ω
Off-Channel Leakage Current (Figure 8)	I _{off}	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel, V _{DD} =15V		±0.05	±100	nA
Capacitance, Switch I/O	C _{I/O}	Inhibit = V _{DD}		10		pF
Capacitance, Common O/I	C _{O/I}	Inhibit = V _{DD}		17		pF
Capacitance, Feedthrough (Channel Off)	C _{I/O}	Pins Not Adjacent Pins Adjacent		0.15 0.47		pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

* For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See second page of this data sheet.)

ELECTRICAL CHARACTERISTICS*

($C_L = 50\text{pF}$, $T_a = 25^\circ\text{C}$, $V_{EE} \leq V_{SS}$, unless otherwise indicated.)

PARAMETER	SYMBOL	$V_{DD} - V_{EE}$ Vdc	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
Propagation Delay Times (Figure 4) Switch Input to Switch Output ($R_L = 10\text{ k}\Omega$)	t_{PLH} , t_{PHL}	5.0	t_{PLH} , $t_{PHL} = (0.17\text{ ns/pF}) C_L + 16.5\text{ ns}$		25	65	ns
		10	t_{PLH} , $t_{PHL} = (0.08\text{ ns/pF}) C_L + 4.0\text{ ns}$		8.0	20	
		15	t_{PLH} , $t_{PHL} = (0.06\text{ ns/pF}) C_L + 3.0\text{ ns}$		6.0	15	
Inhibit to Output	t_{PHZ} , t_{PLZ} t_{PZH} , t_{PZL}	5.0	$(R_L = 10\text{ k}\Omega, V_{EE} = V_{SS})$ Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level		275	550	ns
		10		140	280		
		15		110	220		
Control Input to Output	t_{PLH} , t_{PHL}	5.0	$R_L = 10\text{ k}\Omega, V_{EE} = V_{SS}$		300	600	ns
		10		120	240		
		15		80	160		
Second Harmonic Distortion		10	$R_L = 10\text{ k}\Omega, f = 1\text{ kHz}, V_{in} = 5\text{ V}_{PP}$		0.07		%
Bandwidth (Figure 5)	BW	10	$R_L = 1\text{ k}\Omega, V_{in} = 1/2 (V_{DD} - V_{EE})\text{ p-p},$ $C_L = 50\text{ pF}, 20\text{ Log } (V_{out}/V_{in}) = -3\text{ dB}$		17		MHz
Off Channel Feedthrough Attenuation (Figure 5)		10	$R_L = 1\text{ k}\Omega, V_{in} = 1/2 (V_{DD} - V_{EE})\text{ p-p}$ $f_{in} = 55\text{ MHz}$		-50		dB
Channel Separation (Figure 6)		10	$R_L = 1\text{ k}\Omega, V_{in} = 1/2 (V_{DD} - V_{EE})\text{ p-p}$ $f_{in} = 3.0\text{ MHz}$		-50		dB
Crosstalk, Control Input to Common O/I (Figure 7)		10	$R_1 = 1\text{ k}\Omega, R_L = 10\text{ k}\Omega$ Control $t_{TLH} = t_{THL} = 20\text{ ns}, \text{Inhibit} = V_{SS}$		75		mV

* The formulas given are for the typical characteristics only at 25°C .

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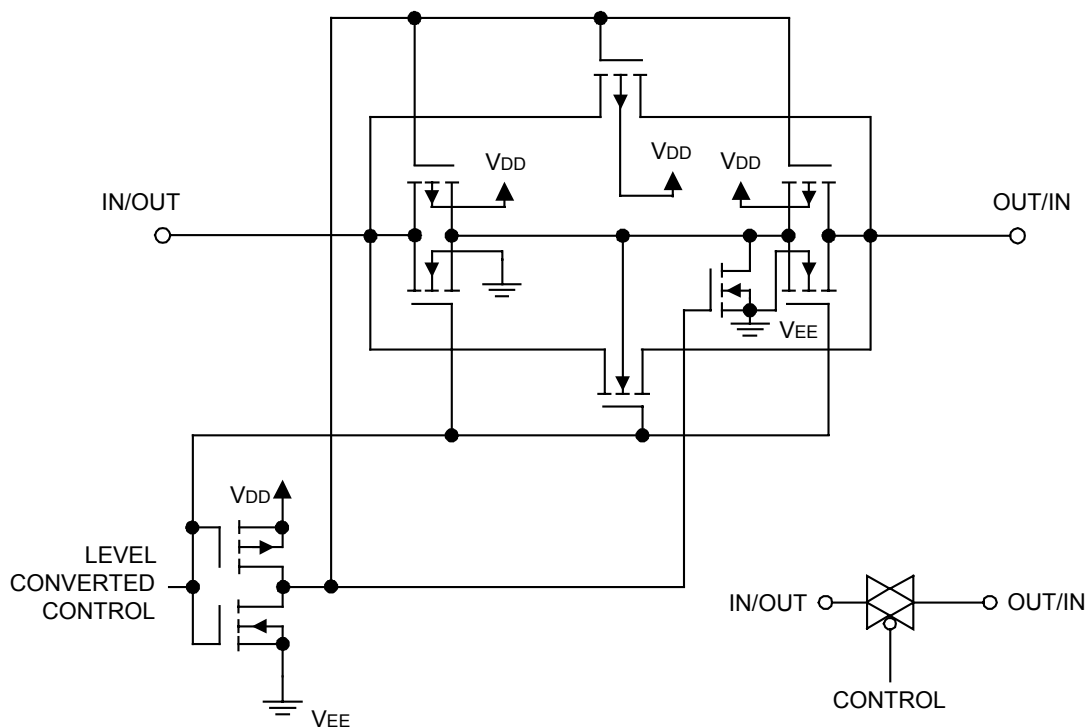


Figure 1. Switch Circuit Schematic

TRUTH TABLE

Control Inputs			ON Switches			
Inhibit	Select			UTC 4053		
	C	B	A	Z0	Y0	X0
0	0	0	0	Z0	Y0	X0
0	0	0	1	Z0	Y0	X1
0	0	1	0	Z0	Y1	X0
0	0	1	1	Z0	Y1	X1
0	1	0	0	Z1	Y0	X0
0	1	0	1	Z1	Y0	X1
0	1	1	0	Z1	Y1	X0
0	1	1	1	Z1	Y1	X1
1	x	x	x	None		

x = Don't Care

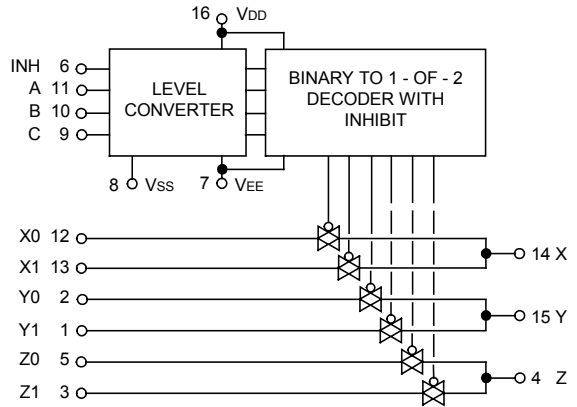
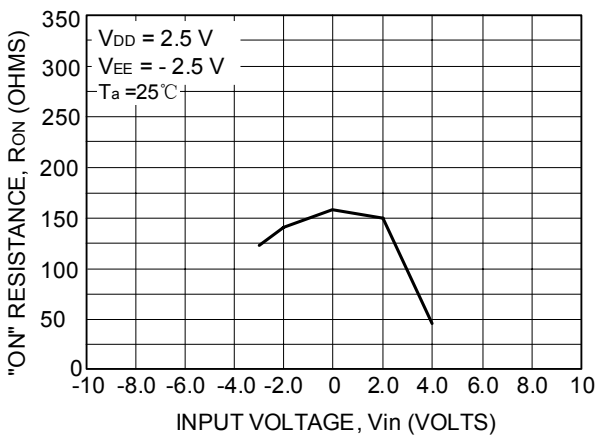
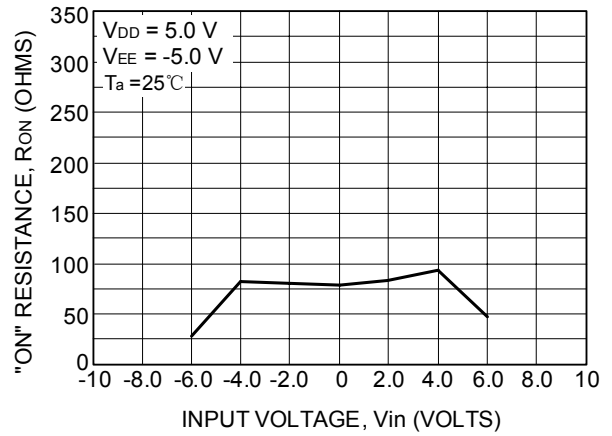
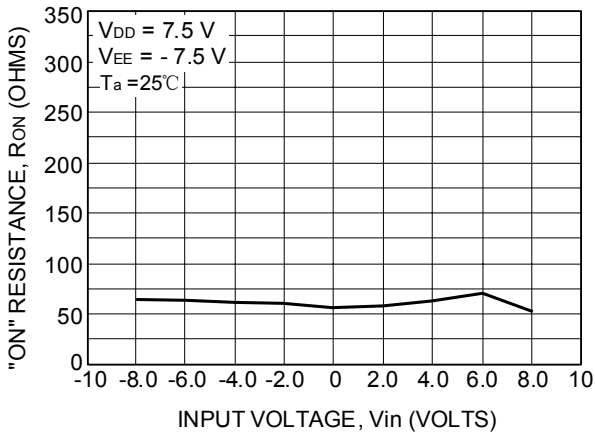


Figure 2. UTC 4053 Functional Diagram



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